H2020-FETHPC-1-2014 ANTAREX-671623

AutoTuning and Adaptivity approach for Energy efficient eXascale HPC systems

Deliverable D6.5: Workshops/Tutorials/Schools on Project Achievements

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Author(s):	João Bispo (UPORTO); Pedro Pinto (UPORTO), João M.P. Cardoso (UPORTO); Jorge Barbosa (UPORTO); Antonio Libri (ETHZ), Jan Martinovič (IT4I), Kateřina Slaninová (IT4I), Martin Golasowski (IT4I), Davide Gadioli (POLIMI), Gianluca Palermo (IT4I), Cristina Silvano (POLIMI).		
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Executive Summary: This is the accompanying report describing the Workshops/Tutorials/Schools organized by the project partners in **Task 6.1 "Dissemination"** with the main focus of to get a higher audience and wider dissemination on the main project achievements, namely:

- Cross-dissemination Workshops, two of them in collaboration with other related HPC projects:
  - HPCAFE-2018 Workshop co-located to European HPC Summit Week 2018 - PRACEdays 2018, Ljubljana, 28 May 1 June 2018
  - EETHPC-2018 Workshop co-located with ISC2018 in Frankfurt, June 28, 2018
  - ANDARE 2018 Workshop co-located with PACT2018, November 1-4, Limassol, Cyprus
- Tutorial: ANTAREX Tutorial given at PACT 2018, Nov. 1-4, Cyprus
- School: PRACE On-demand Event: October 22-23, IT4Innovations, Ostrava, Czech Republic, 2018.

For each dissemination event, the link to the corresponding website is also reported. The links to these events can be easily found from the ANTAREX website: www.antarex-project.eu

Approved and issued by the Project Coordinator: 	**Date:** December 14th, 2018

Project Coordinator: Prof. Dr. Cristina SILVANO – Politecnico di Milano

e-mail: silvano@elet.polimi.it - **Phone:** +39-02-2399-3692- **Fax:** +39-02-2399-3411

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1 Introduction

During the third year of the ANTAREX project we carried out on a number of dissemination events to promote global awareness and cooperation among projects. Herein we present those selected as external dissemination, which are the following.

- **HPCAFE-2018 Workshop:** Workshop on High-Performance Computing Approaches for Monitoring, Exploring, Optimizing and Autotuning, Tuesday, 29 May, 2018, as part of the European HPC Summit Week 2018, 28 May to 01 June, 2018, https://exdci.eu/events/european-hpc-summit-week-2018, Venue: Faculty of Law, University of Ljubljana (Slovenia), University of Ljubljana, Pravna fakulteta/Faculty of Law, Poljanska 2, 1000 Ljubljana, Slovenia. www.fe.up.pt/hpcafe2018.

  Organized jointly with the H2020 FET-HPC projects: ANTAREX, READEX, ALLScale, and ExCAPE.

- **EETHPC-2018 Workshop:** Workshop on Energy Efficiency Tools for High Performance Computing (EETHPC), co-located with the ISC High Performance 2018 (ISC'2018), in Frankfurt, June 28, 2018. Link: http://eethpc.net/

  Organized jointly with members of the H2020 FET-HPC READEX and ANTAREX projects, and the Lawrence Livermore National Laboratory (USA).

- One and a half-day **PRACE On-Demand Event** organized at IT4Innovations, October 22-23, 2018. Link: https://events.it4i.cz/indico/event/14/overview

  Organized by the ANTAREX project and PRACE.

- **ANTAREX Tutorial** (half-day) at The 27th International Conference on Parallel Architectures and Compilation Techniques (PACT18), Limassol, Cyprus, November 3, 2018.

  http://www.antarex-project.eu/pact18

  Organized by the ANTAREX project.

- **ANDARE2018 Workshop** (half-day) at The 27th International Conference on Parallel Architectures and Compilation Techniques (PACT18), Limassol, Cyprus, November 4, 2018. https://www.fe.up.pt/andare2018

  Organized by the ANTAREX project.

The following sections describe in more detail each one of these events.

2 HPCAFE'2018 Workshop

HPCAFE-2018: High-Performance Computing Approaches for Monitoring, Exploring, Optimizing and Autotuning, Tuesday, 29 May, 2018, from 14:30 to 18:30, European HPC Summit Week 2018, 28 May to 01 June, 2018, https://exdci.eu/events/european-hpc-summit-week-2018, Venue: Faculty of Law, University of Ljubljana, Slovenia.

Webpage: http://www.fe.up.pt/hpcafe2018

Overview

The topics of the workshop were focused on the Monitoring, Exploring, Optimizing and Autotuning stages targeting high-performance applications. The program of the event will consist of invited talks, presentations about the projects involved, their approaches, key innovations, and up to date results achieved. The program will also include demonstrations using the tools and the libraries provided by each project and presentations from young researchers (e.g., PhD students involved in those topics). The workshop will close with a session focused on collaboration opportunities.

FET-HPC projects involved:

http://www.allscale.eu	http://www.antarex-project.eu	http://excape-h2020.eu/	http://www.readex.eu

Contacts:

- João MP Cardoso, jmpc@acm.org
- Thomas Fahringer, tf@dps.uibk.ac.at
- Robert Schöne, robert.schoene@tu-dresden.de
- Tom Vander Aa, Tom.VanderAa@imec.be

Program

	Tuesday, 29 May, 2018, Room Sem. 3
14:30-14:35	Opening session
14:35-15:13	**ALLScale: AllScale: On exploiting nested recursive parallelism for performance improvement** by Thomas Fahringer, University of Innsbruck, Austria
15:13-15:51	**The ANTAREX HPC Approach to Help Developers on Program Analysis, Parallelization and Runtime Autotuning** by João MP Cardoso, University of Porto, Portugal
15:51-16:29	**READEX: Runtime Exploitation of Application Dynamism for Energy-efficient eXascale computing** by Umbreen Sabir Mian, Technical University Dresden (TUD)
16:30-17:00	Coffee Break and poster session
17:00-17:38	**The ExCAPE Project: Machine Learning on HPC** by Thomas Ashby, IMEC, Belgium, and Jan Martinovic, IT4Innovations, Czech Republic
17:38-18:25	Open meeting to discuss collaboration opportunities • Opportunities for collaboration • Sharing of tools and applications • Exploitation opportunities • Standardization
18:25-18:30	Closing session

The workshop enabled to the projects involved to cross-disseminate libraries and tools already delivered and planned to be delivered by each project. This might contribute to the use of those libraries and tools by some of the partners of each project.

3 EETHPC-2018 Workshop

The EETHPC-2018 Workshop on Energy Efficiency Tools for High Performance Computing (EETHPC), was co-located with the ISC High Performance 2018 (ISC'2018), in Frankfurt, June 28, 2018. http://eethpc.net/

Overview:

The EETHPC workshop brought together people from different projects that targeted the described research topics. Furthermore, it provided a platform for discussing these subjects with interested researchers, developers, vendors, and users.

During the workshop, the Horizon2020 projects READEX and ANTAREX presented their research results and demonstrate their solutions, including source-to-source compilers, tools, interfaces, and runtime autotuning techniques. The workshop committee invited prestigious scientists from the community to present their current work on energy-efficient HPC. Finally, the workshop will provide a forum for discussing current and upcoming issues in this field.

This half-day workshop included talks by workshop organizers and invited specialists that provided insight into tools and interfaces for energy-efficient computing. During the workshop there was seven talks. In the final timeslot, there was a discussion on existing infrastructure, possibilities and limits of interfaces, and energy efficiency issues.

One of the goals of the EETHPC-2018 Workshop was to provide that participants of the workshop got a broad overview on existing tools and interfaces for energy-efficient computing. The workshop also provided participants with an idea of how hardware interfaces behave under different circumstances and how they can use them effectively. Participants can use this knowledge in the future to avoid re-implementing existing infrastructure and to improve decisions regarding energy-efficient software infrastructure.

Contacts:

- Robert Schöne, robert.schoene@tu-dresden.de, Technische Universität Dresden
- João M.P. Cardoso, jmpc@acm.org, University of Porto
- Barry L. Rountree, rountree4@llnl.gov, Lawrence Livermore National Labs

Program:

Time	Speaker	Affiliation	Topic
02:00 PM	*Robert Schöne*	TU Dresden	Introduction: An Overview on Power Management and Monitoring
02:30 PM	*Roxana Rusitoru*	ARM	Power Saving and Monitoring Features on Hardware Level
03:00 PM	*Rafael Wysocki*	Intel OTC	Linux Power Management Interfaces
03:30 PM	*Alejandro Sanchez*	SchedMD	Slurm's Power Management Capabilities
04:00 PM	Coffee break		
04:30 PM	*Antonio Libri*	MULTITHERMAN	Out-of-band High-Resolution HPC Power and Performance Monitoring Support for Big-Data Analysis
04:50 PM	*Cristina Silvano*	ANTAREX	ANTAREX – Autotuning and Adaptivity for Energy Efficient HPC
05:10 PM	*Andreas Gocht*	READEX	READEX – Tools for Automatized Power Saving in HPC
05:30 PM	Discussion		
06:00 PM	Closing		

4 PRACE On-Demand Event

ANTAREX organized the PRACE On-Demand Event "ANTAREX: Monitoring, Compilation and Autotuning Approach for Energy-Efficient HPC Systems" in October 22 and 23, 2018at VŠB - Technical University of Ostrava, IT4Innovations building, Ostrava, Czech Republic. The event involved presentations and hands-on-approach sessions focused on the ANTAREX DSL, tools, and libraries, and the possibility to access and to run experiments in the Salomon supercomputer[1] of IT4I.

ANTAREX PRACE on-demand event - October 22-23, 2018, Ostrava, Czech Republic

Webpage: https://events.it4i.cz/indico/event/14/overview

Overview

Energy-efficient heterogeneous supercomputing architectures need to be coupled with a radically new software stack capable of exploiting the benefits offered by the heterogeneity at all the different levels (supercomputer, job, node) to meet the scalability and energy efficiency required by Exascale supercomputers. In this school we will start by the background and introduction to relevant topics and then will focus on the ANTAREX approach to solve some of these challenging problems by proposing a disruptive holistic approach spanning all the decision layers composing the supercomputer software stack and exploiting effectively the full system capabilities (including heterogeneity and energy management).

School participants will understand the main challenges and how the ANTAREX project provides a breakthrough approach to express application self-adaptivity at design-time and to runtime manage and autotune applications for green and heterogeneous High Performance Computing (HPC) systems.

The School is specially focused on hands-on-approaches based on representative benchmarks and on the tools provided by the ANTAREX project.

Furthermore, and also very relevant, the topics addressed are especially suited for the next generation of software engineers, software developers and performance engineers (for both HPC and Cloud Computing, but also for high-performance embedded computing). The optimization of applications for heterogeneous distributed computing environments is a relevant topic in general, and we believe that organising the event in cooperation with the ANTAREX project will be a beneficial addition to the PRACE training programme.

Organizers:

IT4Innovations national supercomputing center and ANTAREX project, with support of PRACE (Partnership for Advanced Computing in Europe).

[1] https://docs.it4i.cz/salomon/introduction/

Program

Location: VŠB - Technical University of Ostrava, IT4Innovations building

October 22, 2018

Time	Topic
12:00 - 12:30	Registration
12:30 - 14:00	Lunch
14:00 - 14:30	Opening session and the role of PRACE
14:30 - 15:30	Introduction to Supercomputing Centers and HPC Infrastructures, Visit to IT4Innovations Supercomputing Center
15:30 - 16:00	Coffee Break
16:00 - 17:00	Introduction to Parallel and Distributed Computing at the IT4I Supercomputing Center
17:00 - 18:00	Introduction to Monitoring, Runtime Autotuning, DSL + Source to Source Compilation
19:00 - 21:00	Dinner

October 23, 2018

Time	Topic
09:15 - 09:30	Opening session
09:30 - 10:00	Overview of the ANTAREX Approach
10:00 - 11:00	DSL and Source to Source Compilation: hands-on-approach and the Clava+LARA approach
11:00 - 11:30	Coffee Break
11:30 - 12:30	Runtime Autotuning: hands-on-approach and the mArgot approach
12:30 - 14:00	Lunch
14:00 - 15:00	Energy-Efficiency Run-time: hands-on-approach and the COUNTDOWN approach
15:00 - 16:15	Use of the ANTAREX toolflow and experiments with representative benchmarks and ANTAREX Use Cases
16:15 - 16:45	Coffee Break
16:45 - 17:45	Panel about Open Challenges, Exascale opportunities and challenges, Heterogeneity and the use of Hardware Accelerators, Machine Learning, etc.
17:45 - 18:00	Closing session
19:00 - 21:00	Dinner

5 PACT2018 Tutorial

The ANTAREX team organized on November 3, 2018, a tutorial as an event in the context of the ACM International Conference on Parallel Architectures and Compilation Techniques (PACT18), in Limassol, Cyprus.

Parallel Architectures and Compilation Techniques (PACT18), Limassol, Cyprus November 01-04, 2018

Tutorial: The ANTAREX Approach to Adaptively Optimize and Enforce Extra-Functional Properties on HPC Applications

Date: Nov. 3, 2018

Webpage: http://www.antarex-project.eu/pact18

Abstract

Developing and optimizing applications for energy-efficient HPC systems up to the Exascale era is an extremely challenging problem. They are complex tasks that require mastering several programming languages and tools for performance tuning, which is incompatible with the trend to open HPC infrastructures to a wider range of users. The support of standard languages and APIs is crucial to provide migration paths towards novel heterogeneous HPC platforms as well as to guarantee the ability of developers to work effectively on these platforms. In this tutorial we show how the ANTAREX DSL-based approach allows developers to program and apply strategies (recipes) to applications in the context of extra-functional requirements, such as performance and energy-efficiency. We show our holistic and versatile approach spanning various decision layers composing the supercomputer software stack and exploiting effectively the system capabilities, including heterogeneity and energy management. Specifically, we present the ANTAREX toolflow to enable the definition of energy-efficiency, performance, and adaptivity strategies as well as their enforcement at runtime through application autotuning and resource and power management. Through representative case studies and a hands-on-approach, we show how the ANTAREX toolflow can effectively assist various development/optimization stages, including application analysis and profiling, code transformations and parallelization, and integration of monitoring and runtime autotuning.

Program

Time	Nov. 3rd, 2018
14:30-14:40	**Opening session** *by Cristina Silvano and João MP Cardoso*
14:40-15:00	**Overview of the ANTAREX Approach** *by Cristina Silvano, POLIMI, Italy*
15:00-15:45	**Monitoring and Control: the ExaMon and Countdown approach** *by Daniele Cesarini, Univ. of Bologna, Italy*
15:45-16:30	**Runtime Autotuning: the mArgot approach** *by Gianluca Palermo and Davide Gadioli, POLIMI, Italy*
16:30-17:00	**Coffee Break and Poster Sessions**
17:00-18:00	**DSL and Source to Source Compilation: hands-on-approach** *by Pedro Pinto and João MP Cardoso, UPORTO, Portugal*
18:00-18:30	**Summary of Lessons Learned and Main ANTAREX Achievements** *by Cristina Silvano, POLIMI, Italy*
18:30-18:35	**Closing session** *by Cristina Silvano and João MP Cardoso*

Names and affiliations of main organizers

- Andrea Bartolini, University of Bologna, Italy, a.bartolini@unibo.it
- João M. P. Cardoso, Universidade do Porto, Portugal, jmpc@fe.up.pt
- Cristina Silvano, Politecnico di Milano, Italy, cristina.silvano@polimi.it
- João Bispo, Faculdade de Engenharia da Universidade do Porto, Portugal, jbispo@fe.up.pt
- Daniele Cesarini, University of Bologna, Italy, daniele.cesarini@unibo.it

Main Topics

- Overview of the ANTAREX Approach: In this time slot we will introduce the ANTAREX goals, its main approach and the main tools developed to achieve those goals.
- Monitoring and Control: the ExaMon and Countdown approach: We will introduce the scalable and flexible ExaMon monitoring framework and the Countdown power management library. We will start by describing the problem of large scale cluster monitoring and energy & power optimization of supercomputing machines. We will then describe our ExaMon framework and how this can lead to automated mechanism to manage the datacenter. Finally we present Countdown and explain how you can use it to reduce the energy footprint of your MPI applications in production without paying execution time overheads.
- Runtime Autotuning: the mARGOt approach: We will introduce runtime autotuning and will present the mARGOt approach for runtime autotuning. We will describe how to use mARGOt in a software application, including the creation of a knowledge database, the kind of application and optimization knobs that can be used, the autotuning schemes and the approaches for searching the space and for dealing with multiple goals.

- DSL and Source to Source Compilation: We will start by presenting the main DSL and compiler features provided by Clava+LARA. We will follow a hands-on-approach and the use of simple, but representative, examples to show how the compiler is able to transform code, to automatically parallelize C/C++ code using OpenMP directives, to expose software and optimization knobs for autotuning, and to integrate other tools and APIs (e.g., the ExaMon API and the mARGOt autotuner).
- Main ANTAREX achievements: We will present the main achievements of the ANTAREX approach and toolflow support considering the two ANTAREX industrial use cases requiring HPC: (1) a biopharmaceutical application for drug discovery; and (2) a self-adaptive navigation system for smart cities.

The exercises will be based on an example application that is relatively simple and known to the audience (e.g., matrix multiplication). We will use the LARA DSL and the Clava source to source compiler to apply increasingly more complex strategies over this initial example, starting with simple instrumentation strategies for measuring performance and energy, to performing design-space exploration and finally control the application with an autotuner.

We will show through a hands-on-approach how the tools and APIs provided by ANTAREX are able to efficiently and effectively help users/developers and how they can complement traditional tool flows.

The tools to be used during the tutorial are available at the following sites:

- Clava, DSL-Controlled C/C++ Source to Source Compiler
- Clava+LARA: Complete working versions for a sample of examples
- mARGOt: Runtime Autotuner
- ExaMon: Monitor for Exascale Computation
- Countdown: Power Capper

6 ANDARE'2018 Workshop

Parallel Architectures and Compilation Techniques (PACT18), Limassol, Cyprus November 01-04, 2018

Workshop: ANDARE2018 Workshop (half-day) at The 27th International Conference on Parallel Architectures and Compilation Techniques (PACT18), Limassol, Cyprus, November 4, 2018.

Webpage: https://www.fe.up.pt/andare2018

Overview

High Performance Computing (HPC) has been traditionally the domain of grand scientific challenges and a few industrial domains such as oil & gas or finance, where investments are large enough to support massive computing infrastructures. Nowadays, HPC is recognized as a powerful technology to increase the competitiveness of nations and their industrial sectors, including small scale but high-tech businesses – to compete, you must compute has become an ubiquitous slogan. However, given the performance, power and energy envelops and the increasingly complexity of each computing node, the conventional compiler and code optimization process is no more adequate and there is the need to move to runtime many decisions and explorations of the vast design space. In this context, runtime adaptivity and runtime autotuning is of paramount importance. Furthermore, reaching exascale poses the additional challenge of significantly limiting the energy envelope, while providing massive increases in computational capabilities which may increase the importance of runtime optimizations.

This workshop intends to be an informal, privileged, forum to present and discuss new ideas, challenges, open issues, and trends regarding autotuning and runtime adaptivity in the context of energy-efficient HPC systems. This includes but not limited to the entire vertical stack ranging from the software components (programming best-practices, tools, compilers, runtime environments, operating-systems) to the hardware and firmware components at support of high level autotuning and runtime adaptivity mechanisms. The workshop intends to bring together practitioners, people from supercomputing centers, and researchers interested on those topics. It is foreseen that the workshop may contribute to encourage collaborations among the participants.

Topic areas:

The workshop will address, but is not limited to, the following topics:

- Holistic approaches for autotuning and runtime adaptivity
- Methods to control the decision layers when targeting computations to HPC systems
- Self-adaptive applications
- Optimizations for energy efficiency
- Frameworks and tools for autotuning

- DSLs for describing autotuning strategies
- Parallel application autotuning
- Matching dynamically program parallelism to platform parallelism
- Runtime adaptivity to variable workloads, resource management and power management
- Monitoring libraries for autotuning
- Machine learning approaches for autotuning
- Autotuning and runtime adaptivity in the context of hardware accelerators using GPUs and/or FPGAs
- Applications showing the advantages of online autotuning in HPC
- Power- and energy-aware job schedulers, runtime systems and operating systems.
- Hardware and architectural support for runtime adaptivity

Organizers

- Andrea Bartolini, Università di Bologna, Italy a.bartolini@unibo.it
- João M. P. Cardoso, Universidade do Porto, Portugal, jmpc@fe.up.pt
- Cristina Silvano, Politecnico di Milano, Italy, cristina.silvano@polimi.it

Program:

Sunday, November 4, 2018	
09:30 - 09:40	**Welcome Session** *by Cristina Silvano (POLIMI, IT), João MP Cardoso (UPORTO, PT)*
09:40 - 10:50	**Invited Talks** **Chair:** Cristina Silvano, POLIMI, IT **Accelerating CNN computation: quantisation tuning and network resizing.** *Alexandre Vieira (1), Frederico Pratas (2),* ***Leonel Sousa*** *(1), Aleksandar Ilic (1)* *(1) INESC-ID, Instituto Superior Técnico, Universidade de Lisboa, PT* *(2) Synopsys* **HERO: an Open-Source Research Platform for HW/SW Exploration of Heterogeneous Manycore Systems** ***Alessandro Capotondi*** *(1), Andreas Kurth (2), Andrea Marongiu (1)* *(1) DEI - University of Bologna, IT* *(2) IIS - ETH Zurich; Switzerland*
10:50 - 11:30	**Coffee Break**
11:30 - 12:50	**Regular Papers + Invited Talk** **Chair:** João MP Cardoso, UPORTO, PT **Performance analysis and autotuning setup of the cuFFT library** ***David Střelák*** *and Jiří Filipovič* **COUNTDOWN - A Run-time Library for Application-agnostic Energy Saving in MPI Communication Primitives** ***Daniele Cesarini****, Andrea Bartolini, Pietro Bonfa, Carlo Cavazzoni and Luca Benini* **Evaluation of NTP / PTP Fine-Grain Synchronization Performance in HPC Clusters** ***Antonio Libri****, Andrea Bartolini, Daniele Cesarini and Luca Benini*
12:50 - 13:00	**Closing Session** *by Cristina Silvano (POLIMI, IT), João MP Cardoso (UPORTO, PT)*
13:00 - 14:30	**Lunch**

7 Conclusions

The dissemination activities reported in this deliverable had three main objectives: (a) to disseminate the ANTAREX toolchain and software libraries throughout HPC communities; (b) to interact with other projects with common interests and in order to share experiences and best practices, to make partners aware of the achievements, and to discuss future collaborations; (c) to educate HPC users and HPC application developers about the ANTAREX approach and its tools and libraries.