REC 2021 Programa

5 e 6 de julho

Dia	Hora	Programa
5 de julho	10:30 - 12:30	**Workshop - "IOb-SoC - a RISC-V SoC for teaching, research and innovation"** Orador: José Teixeira de Sousa
	14:00	Welcome desk Q&A (Presencial - Receção e Registo)
	14:30	Sessão de abertura
	15:00	**Keynote - "FPGAs 101 para Engenheiros Informáticos"** Orador: Nuno Paulino
	16:00	**Sessão Regular 1** Chair: João Bispo Tema: *Reconfigurable Embedded Architectures for On-Board Synthetic-Aperture Radar Processing* Orador: Helena Cruz Tema: *Coprocessador Criptográfico em Hardware para RISC-V* Orador: Pedro Sousa Tema: *Array de Microfones para Localização e Identificação de Fontes Sonoras* Orador: Ivo Marques, Afonso Santos
	17:00	Intervalo - Chat Louge (Presencial - Coffe Break)
	17:30	**Fórum - "Uma FPGA…para quê?"** Moderador: Nuno Paulino Tema: *Scalable Digital Baseband Beamformer for Satellite Reception (PhD Thesis)* Orador: Helder Avelar Tema: *Runtime Management of Heterogeneous Compute Resources in Embedded Systems (MsC Thesis)* Orador: Luís Sousa Tema: *An Exploration of FPGAs as Accelerators for Graph Analysis via High-Level Synthesis (MsC Thesis)* Orador: Pedro Silva Tema: *Concealed Target Tracking using Enhanced Radar Techniques (PhD Thesis)* Orador: Luís Duarte Tema: *Hardware-Accelerated Library for Deep Neural Network Applications (MsC Thesis)* Orador: Luís Crespo Tema: *Tensor-Accelerated CPU for Deep Neural Network Applications (MsC Thesis)* Orador: Jorge Simões
	18:30	Fim do primeiro dia

Dia	Hora	Programa
6 de julho	9:30	**Sessão Regular 2** Chair: João Canas Ferreira Tema: *Ferramenta de edição e configuração de código VHDL* Orador: Nuno Leal Tema: *Towards FPGA learning through a game-based approach* Orador: Miguel Marcelo Tema: *CNN implementation in Resource Limited FPGAs - Key Concepts and Techniques* Orador: José Rosa
	10:30	Intervalo - Chat Louge (Presencial - Coffe Break)
	11:00	**Short Keynotes 1** Tema: *FPGA applications in the validation of high-speed interface IPs* Orador: Davide Pereira (Synopsys) Tema: *FPGAs para Sistemas de Alta Velocidade* Orador: Nelson Arqueiro (Altice Labs) Tema: *FPGAs para Sistemas Embebidos* Orador: Carlos Ribeiro (Twevo)
	12:00	**Painel 1 - "FPGAs na Indústria"** Moderador: Mónica Figueiredo Painel: Davide Pereira (Synopsys), Nelson Arqueiro (Altice Labs), Carlos Ribeiro (Twevo)
	12:30	Intervalo para Almoço
	14:00	**Short Keynotes 2** Tema: *Automatic Selection and Insertion of HLS Directives Via a Source-to-Source Compiler* Orador: Tiago Santos Tema: *A First Look at RISC-V Virtualization from an Embedded Systems Perspective* Orador: Bruno Sá Tema: *On Data Parallelism Code Restructuring for HLS Targeting FPGAs* Orador: João Cardoso

	15:00	**Painel 2 - "FPGAs na Investigação: Novas Direções"** Moderador: João Bispo Painel: Arnaldo Oliveira, Tiago Gomes, José T. de Sousa, Manuel Gericota, Pedro Diniz, Tiago Santos
	16:00	Intervalo - Chat Louge (Presencial - Coffe Break)
	16:30	**Sessão Regular 3** Chair: Mónica Figueiredo
		Tema: *Acceleration of Binary Convolutional Neural Networks in Low-Density SoC FPGAs* Orador: Mário Véstias
		Tema: *Sistemas de Visão Industrial: Biblioteca Genérica de Pré Processamento de Imagem em FPGA* Orador: Diogo Ferreira
		Tema: *On the Design of an Object Detection System using Embedded Reconfigurable Logic: Lessons Learned* Orador: Daniel Granhão, Guilherme Carvalho
	17:30 18:00	Sessão de encerramento (Presencial - Porto de Honra)

Workshop IOb-SoC

Building a System-on-Chip has been a privilege reserved only for large semiconductor companies who have the financial resources to design or license processor and peripheral IP cores and assemble them in an SoC. With the advent of the RISC-V architecture, this scenario has changed. SoC design is being democratized, and free design tools and IP cores are now available from the internet. However, creating an SoC is still a very challenging endeavour, and software frameworks that integrate all the software and hardware components needed can be of great help.

This workshop introduces IOb-SoC, a modular SoC framework for teaching, research and innovation. IOb-SoC can be customised to implement highly specialized SoC with varying degrees of complexity. Its hardware is described in (System-)Verilog and its applications are programmed in C/C++. IOb-SoC is hosted at Github, and the repository includes automation scripts to enable simulation, synthesis and place and route of both FPGA and IC, using both free and commercial tools. At the centre of IOb-SoC lies a RISC-V processor. The PicoRV32 RISC-V processor is provided by default, but IOb-SoC can use other processors. IOb-SoC is released in the public domain under the MIT permissive license. By providing the code publicly and at no charge, IOb-SoC can be used by teachers, researchers, and industrial innovators. The advantage of IOb-SoC is that of being straightforward to set up and quick to grasp. It is also modular and can be customised for applications in different contexts. IOb-SoC is supported in a few FPGA boards from different vendors and in an IC 130nm technology node; it can easily port to new boards or IC technologies.

In this workshop, we will start by simulating a RISC-V SoC running the "Hello World" program. Then we will create a custom SoC that incorporated an additional timer IP core. We will learn how to add hardware and software components to IOb-SoC to create a custom SoC. The system will be simulated using the Icarus Verilog simulator and, time permitting, will be implemented in FPGA.