ASAP'23 Program

Wednesday, July 19, 2023

08:00 - 08:30	**Registration** (in front of room B002 – halfway down FEUP's main corridor)
08:30 - 09:00	**Welcome Session** (Room B032)
09:00 - 10:00	**Keynote Speaker 1** Bioinspired Edge AI Systems Co-Design for Internet of Things ***David Atienza***, EPFL, Switzerland **Chair:** Alexandra Jimborean, University of Murcia, Spain
10:00 - 10:45	**Coffee Break + Poster Session** (Coffee Lounge and adjacent hall halfway down FEUP's main corridor)
10:45 - 12:15	**Session W1: Nominated for Best Paper Award and Poster Pitches** Session Chair: Taha Michael Shahroodi, Technische Universiteit Delft (TU Delft), The Netherlands [Paper Presentation] A Novel FPGA-Based Circuit Simulator for Accelerating Reinforcement Learning-Based Design of Power Converters, *Zhenyu Xu, Miaoxiang Yu, Qing Yang, Yeonho Jeong, Jillian Cai and Tao Wei* [Paper Presentation] Enhancing RISC-V Vector Extension for Efficient Application of Post-quantum Cryptography, *Yifan Zhao, Honglin Kuang, Yi Sun, Zhen Yang, Chen Chen, Jianyi Meng and Jun Han* [Paper Presentation] SONA: An Accelerator for Transform-Domain Neural Networks with Sparse-Orthogonal Weights, *Pierre Abillama, Zichen Fan, Yu Chen, Hyochan An, Qirui Zhang, Seungkyu Choi, David Blaauw, Dennis Sylvester and Hun-Seok Kim* [Poster Pitch] COIN: Combinational Intelligent Networks, *Igor D. S. Miranda, Aman Arora, Zachary Susskind, Josias S. A. Souza, Mugdha P. Jadhao, Luis A. Q. Villon, Diego L. C. Dutra, Priscila M. V. Lima, Felipe M. G. França, Mauricio Breternitz and Lizy K. John* [Poster Pitch] A Heterogeneous Computer Architecture Accelerating Reinforcement Learning-based Design for Silicon Photonic Devices, *Miaoxiang Yu, Zhenyu Xu, Qing Yang, Jillian Cai and Tao Wei* [Poster Pitch] Audio DSP to FPGA Compilation, *Maxime Popoff, Romain Michon, Tanguy Risset, Pierre Cochard, Stéphane Letz, Yann Orlarey and Florent de Dinechin*
12:20 - 13:50	**Lunch** (Coffee Lounge - halfway down FEUP's main corridor)
13:50 - 14:50	**Keynote Speaker 2** Storing Digital Data in Synthetic DNA (and a few other musings) ***Karin Strauss***, Microsoft Research and an Affiliate Professor at the University of Washington, USA **Chair:** Pedro C. Diniz, University of Porto, FEUP, Portugal
14:50 - 15:30	**Session W2: Security and Arithmetic** **Session Chair:** José T. Sousa, University of Lisbon / INESC-ID, Portugal MAYALOK: A Cyber-Deception Hardware Using Runtime Instruction Infusion, *Preet Derasari, Kailash Gogineni and Guru Venkataramani* [Short paper] A Suite of Division Algorithms for Posit Arithmetic, *Raul Murillo, Alberto Antonio Del Barrio and Guillermo Botella*
15:30 - 16:00	**Coffee Break + Poster Session** (Coffee Lounge and adjacent hall halfway down FEUP's main corridor)
16:00 - 17:40	**Session W3: Machine Learning I** **Session Chair:** Bo Zhou, Deutsches Forschungszentrum für Künstliche Intelligenz (DFKI), Germany [Paper Presentation] PreCog: Near-Storage Accelerator for Heterogeneous CNN Inference, *Jiyoung An, Esmerald Aliaj and Sang-Woo Jun* [Paper Presentation] iKnowFirst: An Efficient DPU-assisted Compaction for LSM-Tree-based Key-Value Stores, *Jiahong Chen, Shengzhe Wang, Zhihao Zhang, Suzhen Wu and Bo Mao* [Paper Presentation] Expoiting Subword Permutations to Maximize CNN Compute Performance and Efficiency, *Michael Beyer, Sven Gesper, Andre Guntoro, Guillermo Payá Vayá and Holger Blume* [Paper Presentation] AccMER: Accelerating Multi-agent Experience Replay with Cache Locality-aware Prioritization, *Kailash Gogineni, Yongsheng Mei, Tian Lan, Peng Wei and Guru Venkataramani*
17:45 - 19:00	**Welcome Reception** (Main FEUP's Lawn)

Thursday, July 20, 2023

08:50 - 09:00	**Announcements** (Room B032)
09:00 - 10:00	**Keynote Speaker 3** AI for Computer System Analytics ***Ayse Kivilcim Coskun***, Boston University, USA **Chair:** Francesco Regazzoni, University of Amsterdam, The Netherlands, and Università della Svizzera italiana, Switzerland
10:00 - 10:45	**Coffee Break + Poster Session** (Coffee Lounge and adjacent hall halfway down FEUP's main corridor)
10:45 - 12:30	**Session T1: Tools, Simulation and Test** **Session Chair:** José Nelson Amaral, University of Alberta, Canada [Paper Presentation] FAWS: FPGA Acceleration of Large-Scale Wave Simulations, *Dimitrios Gourounas, Bagus Hanindhito, Arash Fathi, Dimitar Trenev, Lizy John and Andreas Gerstlauer* [Paper Presentation] Boomerang: Physical-aware Design Space Exploration Framework on RISC-V SonicBOOM Microarchitecture, *Yen-Fu Liu, Chou-Ying Hsieh and Sy-Yen Kuo* [Paper Presentation] Supporting RISC-V Performance Counters Through Linux Performance Analysis Tools, *João Mário Domingos, Tiago Rocha, Nuno Neves, Nuno Roma, Pedro Tomás and Leonel Sousa* [Paper Presentation] Co-Design of Algorithm and FPGA for Conditional Independence Test, *Ce Guo, Wayne Luk, Alexander Warren, Joshua Levine and Peter Brookes*
12:30 - 14:00	**Lunch** (Coffee Lounge - halfway down FEUP's main corridor)

14:00 - 15:30	**Session T2: Computer Vision** **Session Chair:** Raul Murillo, Complutense University of Madrid, UCM, Spain [Paper Presentation] FieldHAR: A Fully Integrated End-to-end RTL Framework for Human Activity Recognition with Neural Networks from Heterogeneous Sensors, *Mengxi Liu, Bo Zhou, Zimin Zhao, Hyeonseok Hong, Hyun Kim, Sungho Suh, Vitor Fortes Rey and Paul Lukowicz* [Paper Presentation] FMM-X3D: FPGA-based modeling and mapping of X3D for Human Action Recognition, *Petros Toupas, Dimitrios Tzovaras and Christos Bouganis* [Paper Presentation] GPU Acceleration of Multi-object Tracking with Motion Vector interpolation and Affine Transformation, *Yoshiki Kunimoto, Chang Qiong, Yoshiki Yamaguchi and Tsutomu Maruyama* [Short Paper Presentation] Real-time and approximate iterative optical flow implementation on low-power embedded CPUs, *Maxime Millet, Adrien Cassagne, Nicolas Rambaux and Lionel Lacassagne*
15:30 - 16:00	**Coffee Break + Poster Session** (Coffee Lounge and adjacent hall halfway down FEUP's main corridor)
16:00 - 16:50	**Session T3: Security** **Session Chair:** Gabriel Falcão, Instituto de Telecomunicações, University of Coimbra, Portugal [Paper Presentation] Real-time zero-day Intrusion Detection for Automotive Controller Area Network on FPGAs, *S. Khandelwal and S. Shanker* [Paper Presentation] Resource-Constrained Encryption: extending Ibex with a QARMA Hardware Accelerator, *Mathijs De Kremer, Marco Brohet, Subhadeep Banik, Roberto Avanzi and Francesco Regazzoni*
17:00 - 19:30	**Social Event:** Trip to Porto Downtown and Visit to Port Wine Cellar "Caves Calém" (transportation to and from this event is provided by Bus)
19:30 - 22:30	**Dinner** at the "Caves Cálem" restaurant (transportation from the event is provided with limited stops)

Friday, July 21, 2023

08:50 - 09:00	**Announcements** (Room B032)
09:00 - 10:00	**Keynote Speaker 4** **Sustainable Computer Systems** ***Lieven Eeckhout***, Ghent University, Belgium **Chair:** Alexandra Jimborean, University of Murcia, Spain
10:00 - 10:45	**Coffee Break + Poster Session** (Coffee Lounge and adjacent hall halfway down FEUP's main corridor)
10:45 - 12:30	**Session F1: Hardware Acceleration** **Session Chair:** Sergio Pertuz, Technische Universität Dresden (TUD), Germany [Paper Presentation] SieveMem: A Computation-in-Memory Architecture for Fast and Accurate Pre-Alignment, *Taha Shahroodi, Michael Miao, Mahdi Zahedi, Stephan Wong and Said Hamdioui* [Paper Presentation] An FFT Accelerator Using Deeply-coupled RISC-V Instruction Set Extension for Arbitrary Number of Points, *Shijie Jiang, Yi Zou, Hao Wang and Wanwan Li* [Paper Presentation] FarSlayer: Turnkey Acceleration of Legacy Software on Commodity FPGA Cards, *Esmerald Aliaj, Alberto Krone-Martins, Joshua Garcia and Sang-Woo Jun* [Paper Presentation] An Efficient Accelerator for Nonlinear Model Predictive Control, *Sergio Pertuz, Ariel Podlubne and Diana Goehringer*
12:30 - 14:00	**Lunch** (Coffee Lounge - halfway down FEUP's main corridor)
14:00 - 15:40	**Session F2: Machine Learning II** **Session Chair**: Ce Guo, Imperial College London, UK [Paper Presentation] Oikonomos: An Opportunistic, Deep-Learning Resource-Recommendation System for Cloud HPC, *Jan-Harm Betting, Dimitrios Liakopoulos, Max Engelen and Christos Strydis* [Paper Presentation] HLSDataset: Open-Source Dataset for ML-Assisted FPGA Design using High Level Synthesis, *Zhigang Wei, Aman Arora, Ruihao Li and Lizy John* [Paper Presentation] Efficient 1D Grouped Convolution For PyTorch A Case Study: Fast On-Device Fine-Tuning For SqueezeBERT, *Seyyed Hasan Mozafari, James Clark, Warren Gross and Brett Meyer* [Paper Presentation] SimPyler: A Compiler-based Simulation Framework for Machine Learning Accelerators, *Yannick Braatz, Dennis Sebastian Rieber, Taha Soliman and Oliver Bringmann*
15:40 - 16:10	**Coffee Break** (Coffee Lounge)
16:10 - 16:35	**Closing Session**

Poster Presentations

Poster Session: Wednesday to Friday, July 19-21: 10:00 - 10:45
Session Chairs: João Bispo, University of Porto, FEUP and INESC TEC, Portugal; Nuno Paulino, University of Porto, FEUP and INESC TEC, Portugal

[Poster] A Heterogeneous Computer Architecture Accelerating Reinforcement Learning-based Design for Silicon Photonic Devices, *Miaoxiang Yu, Zhenyu Xu, Qing Yang, Jillian Cai and Tao Wei*
[Poster] Audio DSP to FPGA Compilation, *Maxime Popoff, Romain Michon, Tanguy Risset, Pierre Cochard, Stéphane Letz, Yann Orlarey and Florent de Dinechin*
[Poster] COIN: Combinational Intelligent Networks, *Igor D. S. Miranda, Aman Arora, Zachary Susskind, Josias S. A. Souza, Mugdha P. Jadhao, Luis A. Q. Villon, Diego L. C. Dutra, Priscila M. V. Lima, Felipe M. G. França, Mauricio Breternitz and Lizy K. John*

[Regular paper] *SONA: An Accelerator for Transform-Domain Neural Networks with Sparse-Orthogonal Weights, Pierre Abillama, Zichen Fan, Yu Chen, Hyochan An, Qirui Zhang, Seungkyu Choi, David Blaauw, Dennis Sylvester and Hun-Seok Kim*