HARMONIC DISPLACEMENT OF A PARALLEL-PLATE ELECTROSTATIC ACTUATOR USING A PRE-DISTORTED SINEWAVE OSCILLATOR

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Abstract — Harmonic displacement of a parallel plate electrostatic actuator over a maximum amplitude range limited by pull-in, despite the non-linear voltage-to-displacement function is achieved using a pre-distorted waveform. The approach is implemented in a circuit fabricated in a CMOS process for a frequency range up to 1 kHz and tested on a lateral microstructure fabricated in an epi-poly process. The residual second harmonic content in the harmonic displacement is –20 dB.

Key Words: Parallel-plate electrostatic actuator, non-linear actuator, pre-distorted sinewave oscillator, pull-in.

1. INTRODUCTION

Electrostatic actuators are generally classified into two categories: lateral comb drive actuators and parallel-plate actuators. The lateral comb drive actuator generates a force proportional to the applied voltage squared and is, in a first approximation, independent of the associated lateral displacement of the spring-suspended movable part. In the parallel plate actuator of the same dimensions a larger electrostatic force is generated at the same voltage applied. However this force depends on the voltage squared, divided by the parallel plate spacing squared (i.e. the electrostatic field squared). Moreover, the dynamic range of displacement is limited by pull-in. Frequency selective gain control in a servo-operated accelerometer requires, for an optimum operation [1], an harmonic electrostatic force induced displacement of the seismic mass. A large dynamic range requires relatively large electrostatic forces. Therefore, parallel-plate actuation is to be used with pre-distorted sinewaves. The pre-distortion is to anticipate both the squared relation to the excitation voltage and the dependence on the displacement.

2. SIGNAL ANALYSIS

The shape of the excitation voltages required for obtaining a sinusoidal displacement of a moving electrode in an electrostatic field results from an analysis of the electrostatic forces in an electrostatic transducer and is given by:

\[
V(t) = \frac{1 - \frac{1}{G} + \beta \sin(\omega t)}{1 + \beta \sin(\omega t)}
\]

where \(G\) denotes the gain setting of the system (typically \(G=15\) for high sensitivity) and \(\beta\) the modulation index (typ. \(\beta=14/15\)).

![Figure 1. Actuation voltage and resulting electrode displacement, \(\delta(t)\), using a properly pre-distorted sinewave.](image)
quantization (number of samples per period) of the excitation voltage on the electrode displacement function. The acceptable quantization error is specified using the frequency spectrum, $\delta(\omega)$, in terms of the spurious free dynamic range (SFDR).

System performance critically depends on the quality of the oscillator signal. The design of this Direct Digital Frequency Synthesiser (DDFS) and the use on a typical MEMS structure fabricated in an epi-poly process are discussed in the next sections.

3. DESIGN OF THE DDFS

The DDFS for variable frequency is based on a ramp generator plus a DA converter, as shown schematically in Fig. 2 [2, 3].

![Figure 2](image)

Figure 2. Simplified block diagram of the pre-distorted sinewave oscillator.

The special issue imposed by this application is the non-linear DA conversion. A generic CMOS process is used to allow IC-compatible MEMS post-processing, which does not allow for implementation of a ROM look-up table. A specially designed resistor string and two sets of tap switches are used for forming the proper excitation voltages. Only the part for the phase range in between $0^\circ$ and $180^\circ$ is generated and switching is used to synthesize the entire waveform. The ramp with adjustable increment is generated by repetitive addition of a Frequency Control Word (FCW) in the phase accumulator, as shown in Fig. 3. The four most significant bits are used to drive the DA converter to yield the momentary value of the excitation voltage. In the present circuit $m=20$ bits and a 1 MHz system clock is used to enable the generation of a ramp between 1 Hz and 1 kHz with 1 Hz resolution.

![Figure 3](image)

Figure 3. Structure of the Direct Digital frequency Synthesiser DDFS.

The excitation waveform should be such that the associated displacement gain function is a perfect sine function (see Fig. 1). In terms of frequency diagram, for $\delta(t)=\sin(\omega t)$, the drive voltage should contain a DC offset and an harmonic component at $\omega$.

The number of output bits of the phase accumulator determines the number of samples per period and thus the magnitude of the parasitic harmonic components. The quantization therefore introduces harmonics around the sampling frequency. For 8 samples per period the maximum is at the $7^{th}$ harmonic and is equal to $-16.9$ dB. Similarly 16 and 32 samples per period yield $-23.5$ dB at the $15^{th}$ harmonic and $-29.8$ dB at the $31^{th}$ harmonic respectively. The SFDR increases by 6 dB per doubling of the number of samples per period. More samples could in principle provide the spectral range required for filtering. However, additional filtering of $\delta(\omega)$ is difficult to achieve in the mechanical domain and the entire spectrum has to be considered. A design based on 16 samples per period (SFDR=23.5 dB) is sufficient for the intended
application. Moreover, for larger values mismatch between the resistors in the string is expected to dominate system performance.

Table 1. Resistors values for the intended non-linear function

<table>
<thead>
<tr>
<th>Scaled value</th>
<th>Resistor Configuration</th>
<th>Actual Value</th>
<th>Error [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>16.6818</td>
<td>16/1 + 2/3</td>
<td>16.6667</td>
<td>-0.090</td>
</tr>
<tr>
<td>16.3283</td>
<td>16/1 + 2/3</td>
<td>16.3333</td>
<td>0.031</td>
</tr>
<tr>
<td>3.85473</td>
<td>11/3 + 1/5</td>
<td>3.86667</td>
<td>0.310</td>
</tr>
<tr>
<td>1.26789</td>
<td>3/5 + 2/3</td>
<td>1.26667</td>
<td>-0.097</td>
</tr>
<tr>
<td>0.540711</td>
<td>1/25 + 3/6</td>
<td>0.54000</td>
<td>-0.131</td>
</tr>
<tr>
<td>0.265114</td>
<td>1/12 + 2/11</td>
<td>0.26515</td>
<td>0.0154</td>
</tr>
<tr>
<td>0.134629</td>
<td>1/10 + 1/29</td>
<td>0.13448</td>
<td>-0.109</td>
</tr>
<tr>
<td>0.0588235</td>
<td>1/17</td>
<td>0.0588235</td>
<td>0.000</td>
</tr>
</tbody>
</table>

The next design challenge is the design of a resistor string to define the required quantization levels using unit-resistors. The ideal values are scaled to a relative value and subsequently an optimum network of series/parallel connected resistors is designed. Table 1 shows the result (16/1 +2/3 indicates 16 unit resistors in series plus two series connected sets of three unit resistors parallel). The solution is not unique, but yields a deviation from the ideal value smaller than the expected component mismatch.

The planar structure fabricated in silicon using micromachining techniques is shown in Fig. 4. The anchor point is shown in the upper-right corner and interdigitated finger electrodes are available for electrostatic actuation and capacitive detection of displacement. Stoppers are included on either side of the free-standing tip to limit the lateral displacement range. Prototypes have been realized in the Bosch epipoly process. Basically an 11 µm thick polysilicon layer is patterned and released in a surface-micromachining-alike process [4, 5].

4. RESULTS AND CONCLUSIONS

Figure 5 shows the 2.1x2.6 mm² die of the DDFS fabricated in CMOS.
Power consumption is 3 mW for the DDFS at a 1 MHz clock frequency and 0.8 mW for the resistor string at 5V.

Figure 6 shows the displacement function as calculated from the recorded electrical excitation voltage using accurate modeling of the voltage-to-displacement of the electrostatically driven structure shown. The ideal 2\textsuperscript{nd} harmonic distortion at the given sampling rate and using perfectly selected resistors is at -68 dB. However, due to mismatch the actually achieved suppression (as calculated from the electronic waveform) is limited to 32 dB.

Figure 7 shows the time plot of the capacitively measured displacement function and Fig. 8 the associated spectrum in terms of the output voltage of the charge amplifier used for readout. The ringing at the lower maximum of the displacement function is due to the set-up used for capacitively measuring the displacement. The residual second-order distortion is about -20 dB. The difference with the expected limit at -33dB is probably due to the non-linearity of the squeeze-film damping. An improved design with further emphasis on matching considerations of parallel-connected resistors in the string and a modification in the measurement set-up are forthcoming.

Figure 8, Frequency spectrum of the displacement function when driving the actuator with a 16 Hz pre-distorted waveform.

5. REFERENCES