The IEEE 1149.4 std for mixed-signal test

Projecto para a Testabilidade
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[text adapted from the course by José Martins Ferreira]
The IEEE 1149.4 standard for mixed signal test

- Test of Simple Interconnects
The IEEE 1149.4 standard for mixed signal test

• Discrete Component Testing
  (Two line method)

\[
R = \frac{V_1 - V_2}{I}
\]

Parker, McDermid, Oresjo
"Structure and Metrology for an Analog Testability Bus", ITC 93

The IEEE 1149.4 standard for mixed signal test

• Discrete Component Testing
  (Single line method)

\[
R = \frac{2V_{12} - V_{11} - 2V_{22} + V_{21}}{I}
\]

Lu, Mao, Dandapani, Gulati
"Structure and Metrology for a Single-wire Analog Testability Bus", ITC 94
The IEEE 1149.4 standard for mixed signal test

- The power supply based method

\[ I_{DDT} = I_{DD0} + \Delta I \]

\[ R = \frac{V_1 - V_2}{\Delta I} \]

The IEEE 1149.4 standard for mixed signal test

- The 1149.4 std defines an extension to 1149.1, to which it adds:
  - An analogue test port (ATAP) with two pins (AT1, AT2)
  - An internal analogue test bus (AB1, AB2)
  - A test bus interface circuit (TBIC)
  - The analogue boundary modules (ABM)
IEEE 1149.4: The TBIC and the ABMs

- Interconnect and parametric tests can be carried out through the ABMs
- Analogue test signals may be routed from/to the analogue pins to/from the ATAP through the TBIC and the ABMs
- The TBIC and the ABM comprise a switching structure and a control structure

The test bus interface circuit (TBIC)

- The TBIC defines the interconnections between the ATAP (AT1 and AT2) and the internal analogue test bus (at least two lines, AB1 and AB2)
- The TBIC comprises a switching structure and a control structure
### TBIC: The switching structure

![Diagram of the switching structure](image)

### TBIC: Switching structure patterns

<table>
<thead>
<tr>
<th>Pattern</th>
<th>Switch conditions</th>
<th>Connections and functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0</td>
<td>0 0 0 0 0 1 1 1 1</td>
<td>AB1/2 disconnected from clamp, mission mode</td>
</tr>
<tr>
<td>P1</td>
<td>0 0 0 0 0 1 0 1 0</td>
<td>AB1 connected to AT1 and/or AT2, connected to AT2; disconnected bus clamped, PROBE, INTEST, Extended interconnect testing in EXTEST</td>
</tr>
<tr>
<td>P2</td>
<td>0 0 0 0 1 1 0 0 0</td>
<td>Logic signals applied to AT1/2 = 00</td>
</tr>
<tr>
<td>P3</td>
<td>0 0 0 0 1 1 1 1 1</td>
<td>Logic signals applied to AT1/2 = 01, Internal buses clamped, Simple interconnect testing (EXTTEST)</td>
</tr>
<tr>
<td>P4</td>
<td>0 0 1 1 0 0 0 0 1</td>
<td>AT1/2 = 10</td>
</tr>
<tr>
<td>P5</td>
<td>1 0 0 0 0 0 1 1 1</td>
<td>AT1/2 = 11</td>
</tr>
<tr>
<td>P6</td>
<td>1 1 0 0 1 1 1 1 1</td>
<td>AT1/2 = 10</td>
</tr>
<tr>
<td>P7</td>
<td>1 1 0 0 1 1 1 1 1</td>
<td>AT1/2 = 11</td>
</tr>
<tr>
<td>P8</td>
<td>0 0 0 0 0 1 0 1 0</td>
<td>AT1 connected to A2 via internal buses, Characterisation (in EXTEST)</td>
</tr>
<tr>
<td>P9</td>
<td>0 0 0 0 0 1 0 1 0</td>
<td>AT1 connected to A2 via internal buses, Characterisation (in EXTEST)</td>
</tr>
</tbody>
</table>
Switching assignments for defined instructions (TBIC)

<table>
<thead>
<tr>
<th>Clock/Clear</th>
<th>EXTEST</th>
<th>CLAMP</th>
<th>UNTEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>P0</td>
<td>P0</td>
<td></td>
</tr>
<tr>
<td>001</td>
<td>P1</td>
<td>P1</td>
<td></td>
</tr>
<tr>
<td>010</td>
<td>P2</td>
<td>P2</td>
<td></td>
</tr>
<tr>
<td>011</td>
<td>P3</td>
<td>P3</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>P4</td>
<td>*</td>
<td>100</td>
</tr>
<tr>
<td>101</td>
<td>P5</td>
<td>*</td>
<td>101</td>
</tr>
<tr>
<td>110</td>
<td>P6</td>
<td>*</td>
<td>110</td>
</tr>
<tr>
<td>111</td>
<td>P7</td>
<td>*</td>
<td>111</td>
</tr>
</tbody>
</table>

TBIC: Control structure

Control logic

Parallel output

Serial input

Parallel input

Inputs available to the user

V_{TH}

Switching structure comparators

Mode

Parallel output

Serial output

Serial output

Parallel input

mux

C/S

Parallel output

DBM

ABM

(AB1, AB2)

BST infrastructure (except the BST register)

TDO

TDI

TMS

TCK

AT1

AT2
The analogue boundary modules (ABM)

- The ABMs in the analogue pins extend the test functions made available by the DBMs
- All test operations combine digital (via TAP) and analogue test “vectors” (via ATAP)
- Each ABM comprises a switching structure and a control structure

ABMs: Switching structure
ABMs: Switching structure patterns (1)

<table>
<thead>
<tr>
<th>Pattern</th>
<th>SB</th>
<th>SH</th>
<th>SL</th>
<th>SG</th>
<th>SB1</th>
<th>SB2</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P1</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P2</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>P3</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P4</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P5</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P6</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>P7</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P8</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P9</td>
<td>0</td>
<td>0</td>
<td>C</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Pin state
- Completely isolated (CC state).
- Monitored by AB2.
- Connected to AB1.
- Connected to AB2.
- Connected to V0, monitored by AB2.
- Connected to V0 and AB1.
- Connected to V0 and AB1, monitored by AB2.
- Connected to V0.
- Connected to V0, monitored by AB2.

Main testing conditions for analogue measurements

ABMs: Switching structure patterns (2)

<table>
<thead>
<tr>
<th>Pattern</th>
<th>SB</th>
<th>SH</th>
<th>SL</th>
<th>SG</th>
<th>SB1</th>
<th>SB2</th>
</tr>
</thead>
<tbody>
<tr>
<td>P12</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P13</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>P14</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P15</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>P16</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>P17</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>P18</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Pin state
- Connected to V0 and AB1.
- Connected to V0 and AB2.
- Connected to V0.
- Connected to V0 and AB1.
- Connected to V0 and AB1, monitored by AB2.
- Connected to V0.
- Connected to V0, monitored by AB2.
- Connected to core; isolated from all test circuits.
- Connected to core; monitored by AB2.
- Connected to core; monitored by AB1.
- Connected to core and AB1, monitored by AB2.

Normal mission operation: pin connected to core only.
ABMs: Switching pattern requirements

<table>
<thead>
<tr>
<th>Code</th>
<th>C/D</th>
<th>ENTEST</th>
<th>CLAMP</th>
<th>PROBE</th>
<th>ENTEST</th>
<th>CLAMP</th>
<th>PROBE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>P1</td>
<td>P16</td>
<td>P17</td>
<td>P9</td>
<td>P1</td>
<td>P19</td>
<td>P7</td>
</tr>
<tr>
<td>0001</td>
<td>P2</td>
<td>P18</td>
<td>P10</td>
<td>P10</td>
<td>P1</td>
<td>P10</td>
<td>P7</td>
</tr>
<tr>
<td>0010</td>
<td>P3</td>
<td>P19</td>
<td>P11</td>
<td>P11</td>
<td>P1</td>
<td>P11</td>
<td>P7</td>
</tr>
<tr>
<td>0011</td>
<td>P4</td>
<td>*</td>
<td>P12</td>
<td>*</td>
<td>P1</td>
<td>P12</td>
<td>*</td>
</tr>
<tr>
<td>0100</td>
<td>P5</td>
<td>*</td>
<td>P13</td>
<td>*</td>
<td>P1</td>
<td>P13</td>
<td>*</td>
</tr>
<tr>
<td>0101</td>
<td>P6</td>
<td>*</td>
<td>P14</td>
<td>*</td>
<td>P1</td>
<td>P14</td>
<td>*</td>
</tr>
<tr>
<td>0110</td>
<td>P7</td>
<td>*</td>
<td>P15</td>
<td>*</td>
<td>P1</td>
<td>P15</td>
<td>*</td>
</tr>
</tbody>
</table>

ABMs: Control structure

Control logic

Parallel input

Serial input

Switching structure comparator

V_TH

Mode

Serial output

Parallel output

ABM

BST infrastructure (except the BST register)

TDI

TCK

TMS

TBIC

C/S

Pin

Parallel output

mux

Serial input

SD

SH

SH

SB2

ABMs: Control structure
The 1149.4 register structure

- The 1149.4 register structure is entirely digital and identical to the corresponding 1149.1 structure.

The PROBE instruction

- The IEEE 1149.4 std defines a fourth mandatory instruction called PROBE:
  - The selected data register is the BS register
  - One or both of the ATAP pins connect to the corresponding AB1/AB2 internal test bus lines
  - Analog pins connect to the core and to AB1/AB2 as defined by the ABM 4-bit control word
  - Each DBM operates in transparent mode
Analog test operations

- Principle of operation:
  - The analog signal is applied to AT1 and the analog response is observed in AT2
  - With AT1 connected to AB1, the analog signal may be routed to the internal circuitry or to an analog output pin
  - Analog responses from the internal circuitry or from an analog input pin are routed to AB2, and observed in AT2

Observability of analog (input / output) pins

- The signal present at any analog (input / output) pin may be observed at AT2, with (or without) the core connected to the pin
Controllability of analog (input / output) pins

- The signal present at any analog (input / output) pin may be driven from AT1, regardless of the signal present at the analog input.

Impedance measurement between pin and ground

\[ Z_D = \frac{V_T}{I_T} \text{ if:} \]

- \[ Z_V \gg Z_{S6} + Z_{SB2} \]
- \[ Z_V + Z_{S6} + Z_{SB2} \gg Z_D \]
Interconnect testing with 1149.4

Functional description of a basic “1149.4 component”

• The core circuitry is restricted to
  – A voltage follower
  – A logic inverter
• The required 1149.4 infrastructure should only support the mandatory instructions
Summary description of the 1149.4 infrastructure

- Instruction codes (8-bit):
  - EXTEST: $00
  - SAMPLE / PRELOAD: $02
  - PROBE: $01
  - BYPASS: $FF

- Boundary scan register (TDI-TDO, 14-bit):
  - TBIC (4-bit), ABM analog input (4-bit), ABM analog output (4-bit), DBM digital input (1-bit), DBM digital output (1-bit)